



# Intel® Celeron® M Processor on 90 nm Process for Embedded Applications

Thermal Design Guide

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*April 2005*



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# Contents

<b>1.0</b>	<b>Introduction</b>	6
1.1	Document Goals	6
1.2	Document Scope	6
1.3	Document References	6
1.4	Glossary of Terms and Acronyms	7
<b>2.0</b>	<b>Design Guidelines</b>	8
2.1	Mechanical Guidelines	8
2.1.1	Processor Package	8
2.1.2	Volumetric Constraint Zones	15
2.2	Thermal Guidelines	19
2.2.1	Processor Power	20
2.2.2	Thermal Diode	20
2.2.3	Intel Thermal Monitor	21
2.2.4	Power Density and Non-Uniform Heating	22
2.2.5	Thermal Solution Requirements	22
2.2.6	Recommended Heat Sink Designs	23
2.2.7	Thermal Interface Material (TIM)	30
2.2.8	Recommended Thermal Solution Attachment Method	31
2.2.9	Intel® Celeron® M Processor Thermal Test Vehicle	31
<b>3.0</b>	<b>Third-Party Vendor Enabled Active Heat Sinks</b>	32
3.1	Applications	32
3.1.1	EEP-N41ES-02 and EEB-N41ES-02	32
3.1.2	EEP-N41CS-01 and EEB-N41CS-01	33
3.1.3	EEP-N41SS-01 and EEB-N41SS-01	34
3.2	Thermal Interface Material and Considerations	35
<b>4.0</b>	<b>Vendor Information</b>	36
<b>A</b>	<b>Heat Sink Mechanical Drawings</b>	37

## Tables

1	Document References	6
2	Glossary of Terms and Acronyms	7
3	Micro-FCBGA Package Dimensions	11
4	Micro-FCPGA Package Dimensions	14
5	Thermal Specifications for the Intel® Celeron® M Processor and Ultra Low Voltage Intel® Celeron® M Processor	20
6	Aluminum Active Heat Sink Thermal Performance	33
7	Active Copper Heat Sink Thermal Performance	34
8	Copper Active Heat Sink Thermal Performance	35
9	Vendor Contact Information†	36

## Figures

1	Micro-FCBGA Package Top and Bottom Isometric View .....	9
2	Micro-FCBGA Package Top and Side View .....	9
3	Micro-FCBGA Package Bottom View .....	10
4	Micro-FCPGA Package Top and Bottom Isometric View .....	11
5	Micro-FCPGA Package—Bottom View .....	12
6	Micro-FCPGA Package—Top and Side View .....	13
7	Recommended PCB Volumetric Constraint Zone for Intel® Celeron® M processor Ultra Low Voltage in the Single-slot CompactPCI* Form Factor .....	15
8	Intel® Celeron® M processor Ultra Low Voltage Recommended PCB Volumetric Constraint Zone for the AdvancedMC* on an AdvancedTCA* Carrier Card (Primary Side) .....	16
9	Intel® Celeron® M processor Ultra Low Voltage Recommended PCB Volumetric Constraint Zone for the AdvancedMC* on an AdvancedTCA* Carrier Card (Secondary Side) ..	17
10	Single-slot CompactPCI* Form Factor Recommended PCB Volumetric Constraint Zone for the Intel® Celeron® M Processor in the micro-FCBGA Package .....	18
11	Single-slot CompactPCI* Form Factor Recommended PCB Volumetric Constraint Zone for the Intel® Celeron® M Processor in the micro-FCPGA Package .....	19
12	Thermal Resistance Values for the Intel® Celeron® M Processor 370 at Various Local Ambient Operating Temperatures .....	23
13	Intel® Celeron® M Processor Copper Base, Aluminum Fin Heat Sink #1 (EID-BAN24-CUALC-001SS) Thermal Performance Curve .....	24
14	Intel® Celeron® M Processor Copper Base, Aluminum Fin Heat Sink #2 (EID-BAN24-CUALC-002SS) Thermal Performance Curve .....	25
15	Celeron® M Processor ULV 373 Extruded Aluminum Heat Sink #1 (EID-BAN15-ALX-003SS) Thermal Performance Curve.....	26
16	Intel® Celeron® M Processor Ultra Low Voltage 373 Extruded Aluminum Heat Sink #2 (EID-LPT13-ALX-003) Thermal Performance Curve .....	27
17	Reference Heat Sink for the Celeron® M Processor Ultra Low Voltage 373 for the AdvancedMC* on an AdvancedTCA* Carrier Card, Thermal Performance Curve .....	29
18	Heat Sink Orientation Relative to Airflow Direction .....	30
19	Active Aluminum Heat Sink, EEP-N41ES-02 and EEB-N41ES-02 .....	32
20	Active Copper Heat Sink, EEP-N41CS-01 and EEB-N41CS-01 .....	33
21	Copper Active Heat Sink, EEP-N41SS-01 and EEB-N41SS-01 .....	34
22	Intel® Celeron® M Processor in the Micro-FCBGA Package Heat Sink #1 (EID-BAN24-CUALC-001SS) .....	37
23	Intel® Celeron® M Processor in the Micro-FCPGA Package Heat Sink #2 (EID-BAN24-CUALC-002SS) .....	38
24	Ultra Low Voltage Intel® Celeron® M Processor—Extruded Aluminum Heat Sink #1 (EID-BAN15-ALX-003SS).....	39
25	Ultra Low Voltage Intel® Celeron® M Processor—Extruded Aluminum Heat Sink #2 (EID-LPT13-ALX-003) .....	40
26	Reference Heat Sink for the Ultra Low Voltage Intel® Celeron® M Processor in the AdvancedMC* Form Factor (Page One).....	41
27	Reference Heat Sink for the Ultra Low Voltage Intel® Celeron® M Processor in the AdvancedMC* Form Factor (Page Two).....	42
28	Active Heat Sink Volumetric Constraint Zone (Primary Side).....	43
29	Active Heat Sink Volumetric Constraint Zone (Secondary Side).....	44



## Revision History

Date	Revision	Description
April 2005	001	Initial public release of this document

## 1.0 Introduction

This document describes thermal design guidelines for the Intel® Celeron® M Processor on 90 nm process with 400 MHz front side bus in the Micro Flip Chip Ball Grid Array (micro-FCBGA) package and the Micro Flip Chip Pin Grid Array (micro-FCPGA) package. Detailed mechanical and thermal specifications for this processor may be found in the *Intel® Celeron® M Processor on 90 nm Process Datasheet*.

The information provided in this document is for reference only and additional validation must be performed prior to implementing the thermal designs into final production. The intent of this document is to assist OEMs with the development of thermal solutions for their individual designs. It is the responsibility of each OEM to validate the thermal solution design, including the heat sink, attachment method, and thermal interface material (TIM) with their specific applications.

## 1.1 Document Goals

This document describes the thermal characteristics of the Celeron M processor and provides guidelines for meeting the thermal requirements imposed on uni-processor systems. The thermal solutions presented in this document are specifically designed for applied computing applications in embedded form factors.

## 1.2 Document Scope

This document discusses the thermal management techniques for the Celeron M processor, specifically in embedded computing applications. The physical dimensions and power numbers used in this document are for reference only. Please refer to the processor's datasheet for the product dimensions, thermal power dissipation, and maximum junction temperature. In case of conflict, the data in the datasheet supersedes any data in this document.

## 1.3 Document References

**Table 1. Document References**

Title	Number
<i>Intel® Celeron® M Processor on 90 nm Process Datasheet</i>	303110
<i>Intel® Mobile Processor Micro-FCPGA Socket (mPGA479M) Design Guidelines</i>	298520

## 1.4 Glossary of Terms and Acronyms

**Table 2. Glossary of Terms and Acronyms**

Term	Definition
CFM	Cubic feet per minute
LFM	Linear feet per minute
PCB	Printed circuit board
$\Psi_{JA}$	Junction-to-Ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_J - T_A) / \text{Total Package Power}$ . Note: Heat source must be specified for $\Psi$ measurements.
$\Psi_{JS}$	Junction-to-Sink thermal characterization parameter (psi). A measure of the thermal interface material performance using total package power. Defined as $(T_J - T_S) / \text{Total Package Power}$ . Note: Heat source must be specified for $\Psi$ measurements. Also referred to as $\Psi_{TIM}$ .
$\Psi_{SA}$	Sink-to-Ambient thermal characterization parameter (psi). A measure of the heat sink's performance using total package power. Defined as $(T_S - T_A) / \text{Total Package Power}$ . Note: Heat source must be specified for $\Psi$ measurements.
$T_{\text{junction}}$	The measured junction temperature of the processor. Also referred to as $T_J$ .
$T_{\text{junction-max}}$	The maximum junction temperature of the processor, as specified in the processor datasheet. Also referred to as $T_{J\text{-max}}$ .
$T_{LA}$ ( $T_{\text{Local-Ambient}}$ )	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured approximately one inch (25.4 mm) upstream of a passive heat sink, or at the fan inlet of an active heat sink
Thermal Design Power (TDP)	A design point for the processor. OEMs must design thermal solutions that meet TDP and $T_{\text{junction}}$ specifications as specified in the processor's datasheet.
Thermal Interface Material (TIM)	The thermally conductive compound between the heat sink and processor die. This material fills air gaps and voids, and improves the spread of heat from the die to the heat sink.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 inches, 2U equals 3.50 inches, etc.

## 2.0 Design Guidelines

The thermal solutions presented in this document were designed to fit within the maximum component height allowed by certain embedded form factor specifications, including single-slot CompactPCI\* and the Advanced Mezzanine Card (AdvancedMC\*) for the AdvancedTCA\* form factor. The thermal solutions may be valid for other form factors; however, individual applications must be modeled, prototyped, and verified.

In some cases, prototype parts have been fabricated for verification testing. It is important to note that the thermal verification information described in this document is not adequate for statistical purposes. The intent of testing was only to verify that the thermal components were performing within reasonable expectations, based on computer modeling and component specifications.

## 2.1 Mechanical Guidelines

### 2.1.1 Processor Package

The Celeron M processor is available in the 479-ball Micro-Flip Chip Ball Grid Array (micro-FCBGA) package and the 478-pin Micro-Flip Chip Pin Grid Array (micro-FCPGA) package technology. The Celeron M processor Ultra Low Voltage (ULV) is only available in the micro-FCBGA package. Detailed mechanical specifications for the processor may be obtained from the processor datasheet.

Figure 1, Figure 2 and Figure 3 show different views of the micro-FCBGA package; dimensions are provided in Table 3. Figure 4, Figure 5 and Figure 6 show different views of the micro-FCPGA package; dimensions in Table 4. Refer to the *Intel® Celeron® M Processor on 90 nm Process Datasheet* for detailed information.

The micro-FCBGA package may have capacitors placed in the area surrounding the die. Since die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short-circuit the capacitors, and possibly damage the device or render it inactive. Consider using an insulating material between the capacitors and any thermal solution to prevent capacitor shorting.



Figure 1. Micro-FCBGA Package Top and Bottom Isometric View

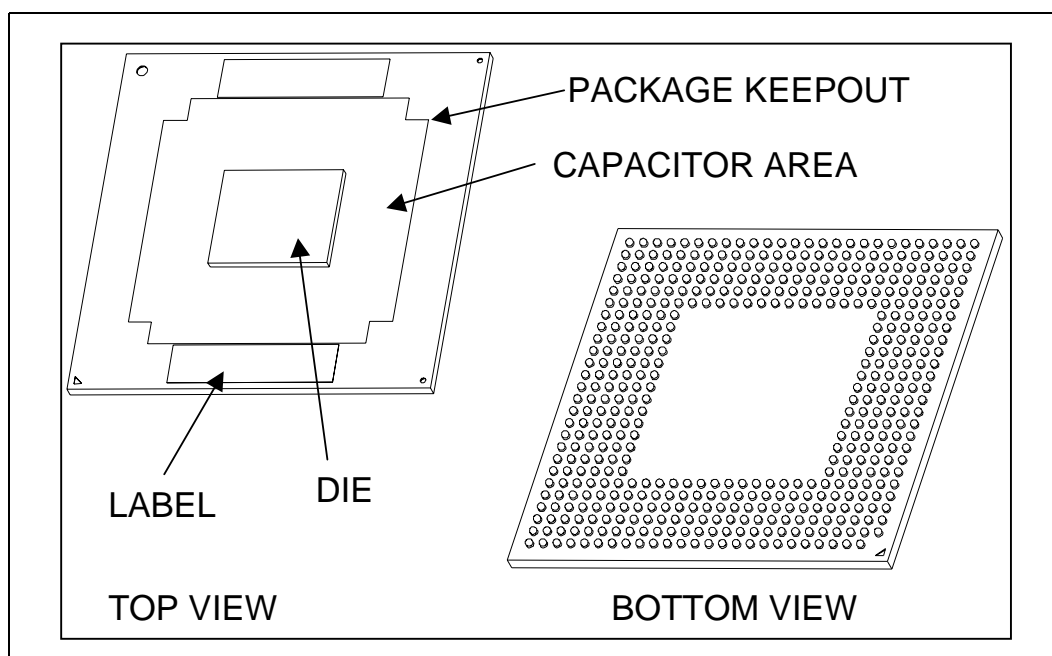


Figure 2. Micro-FCBGA Package Top and Side View

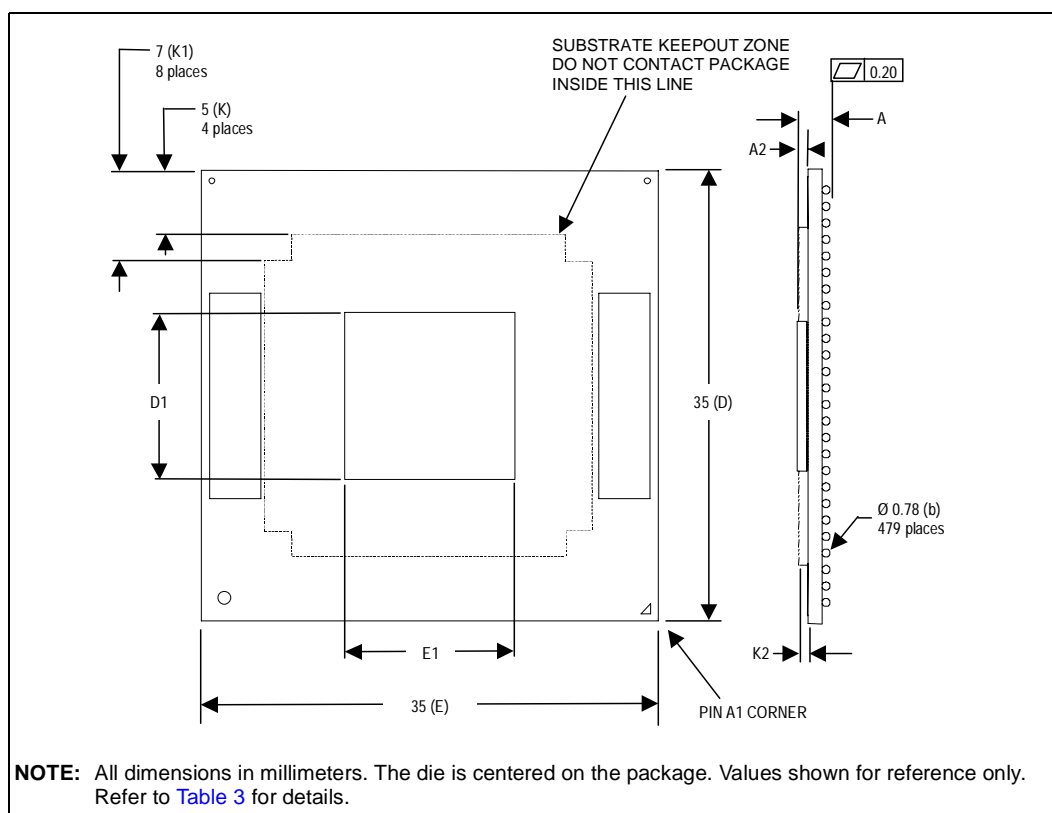
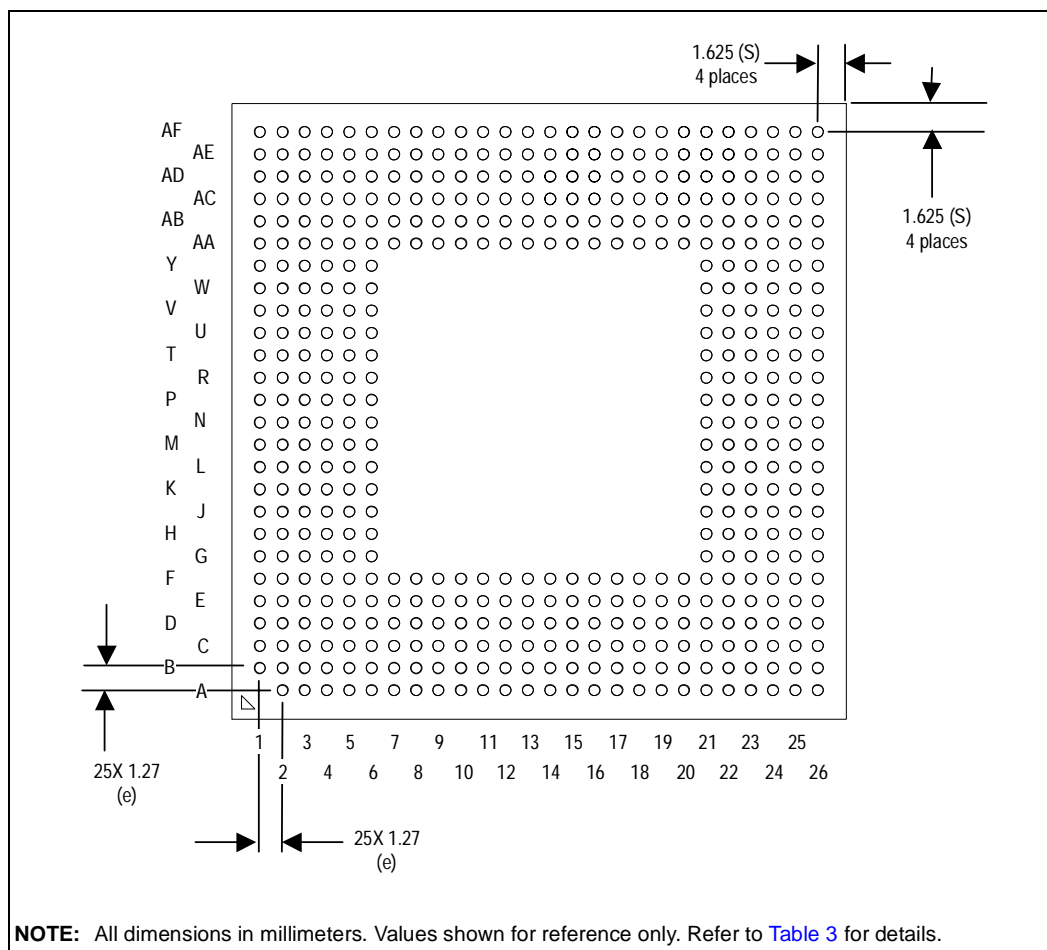


Figure 3. Micro-FCBGA Package Bottom View



**Table 3. Micro-FCBGA Package Dimensions**

Symbol	Parameter	Min	Max	Unit
A	Overall height, as delivered (Refer to Note 1.)	2.60	2.85	mm
A2	Die height	0.82		mm
b	Ball diameter	0.78		mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	12.54		mm
E1	Die width	6.99		mm
e	Ball pitch	1.27		mm
K	Package edge keep-out	5		mm
K1	Package corner keep-out	7		mm
K2	Die-side capacitor height	–	0.7	mm
S	Package edge to first ball center	1.625		mm
N	Ball count	479		each
–	Solder ball co-planarity	0.2		mm
Pdie	Allowable pressure on the die for thermal solution	–	689	kPa
W	Package weight	4.5		g

**NOTE:**

1. Overall height as delivered. Values are based on design specifications and tolerances. This dimension is subject to change based on OEM motherboard design or OEM SMT process.

**Figure 4. Micro-FCPGA Package Top and Bottom Isometric View**

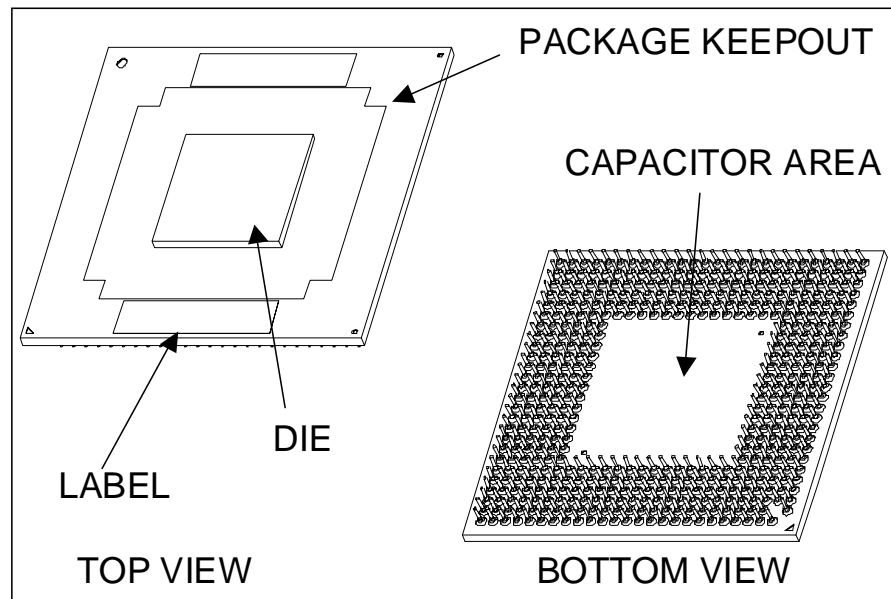


Figure 5. Micro-FCPGA Package—Bottom View

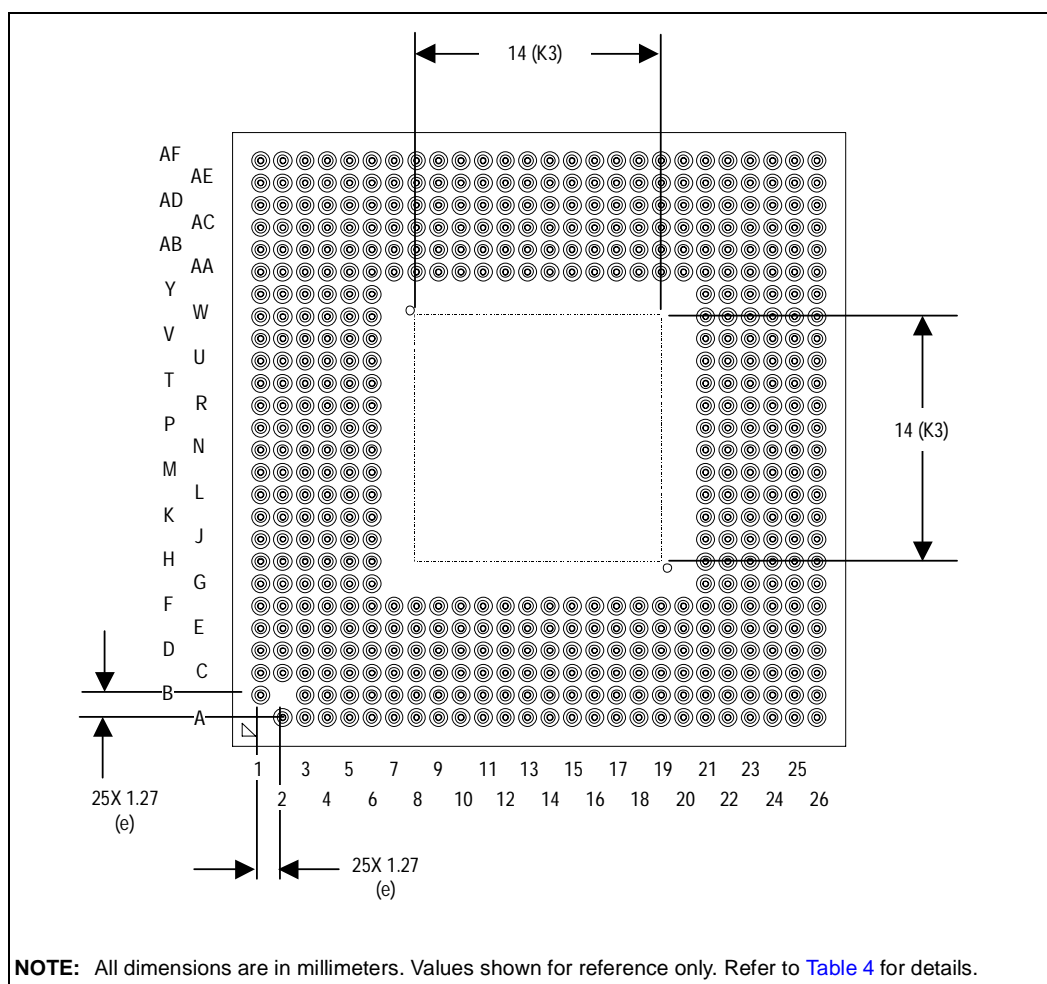


Figure 6. Micro-FCPGA Package—Top and Side View

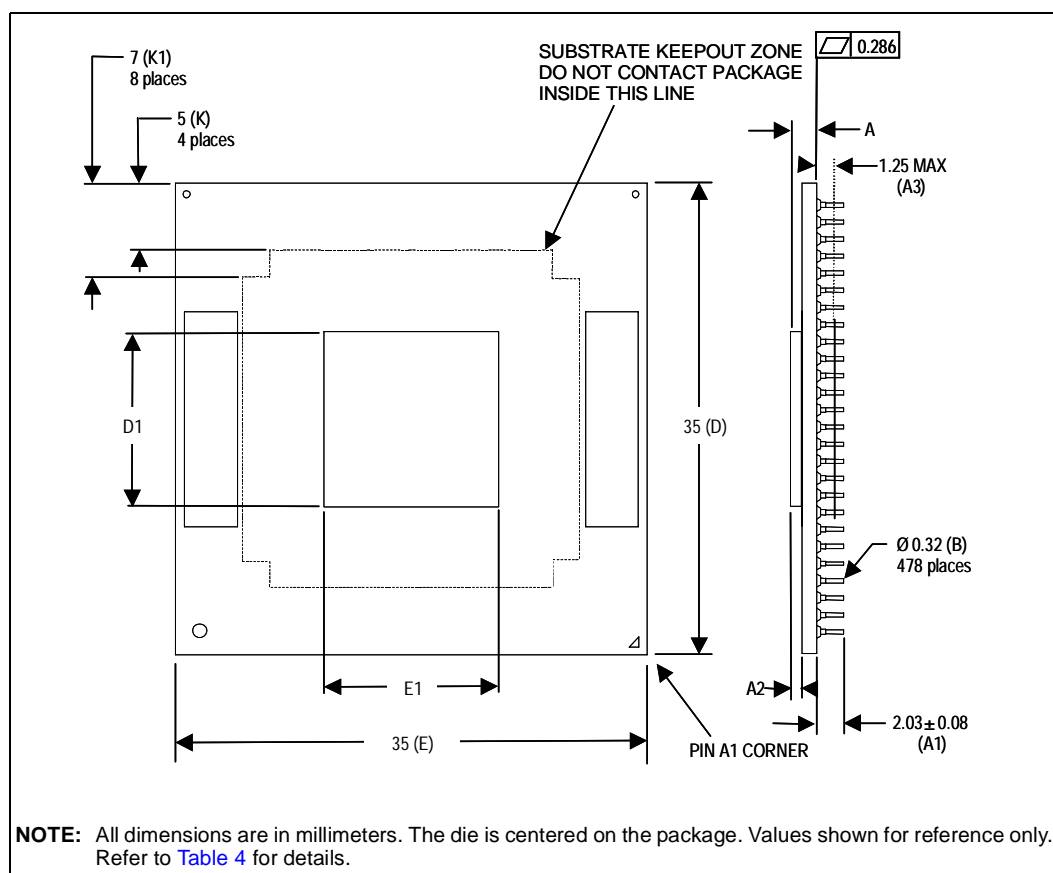


Table 4. Micro-FCPGA Package Dimensions

Symbol	Parameter	Min	Max	Unit
A	Overall height, top of die to package seating plane	1.88	2.02	mm
–	Overall height, top of die to PCB surface, including socket (Refer to <a href="#">Note 1.</a> )	4.74	5.16	mm
A1	Pin length	1.95	2.11	mm
A2	Die height	0.820		mm
A3	Pin-side capacitor height	–	1.25	mm
B	Pin diameter	0.28	0.36	mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	12.54		mm
E1	Die width	6.99		mm
e	Pin pitch	1.27		mm
K	Package edge keep-out	5		mm
K1	Package corner keep-out	7		mm
K3	Pin-side capacitor boundary	14		mm
N	Pin count	478		each
Pdie	Allowable pressure on the die for thermal solution	–	689	kPa
W	Package weight	4.5		g
	Package Surface Flatness	0.286		mm

**NOTE:**

1. Overall height with socket is based on design dimensions of the Micro-FCPGA package with no thermal solution attached. Values are based on design specifications and tolerances. This dimension is subject to change based on socket design, OEM motherboard design or OEM SMT process.

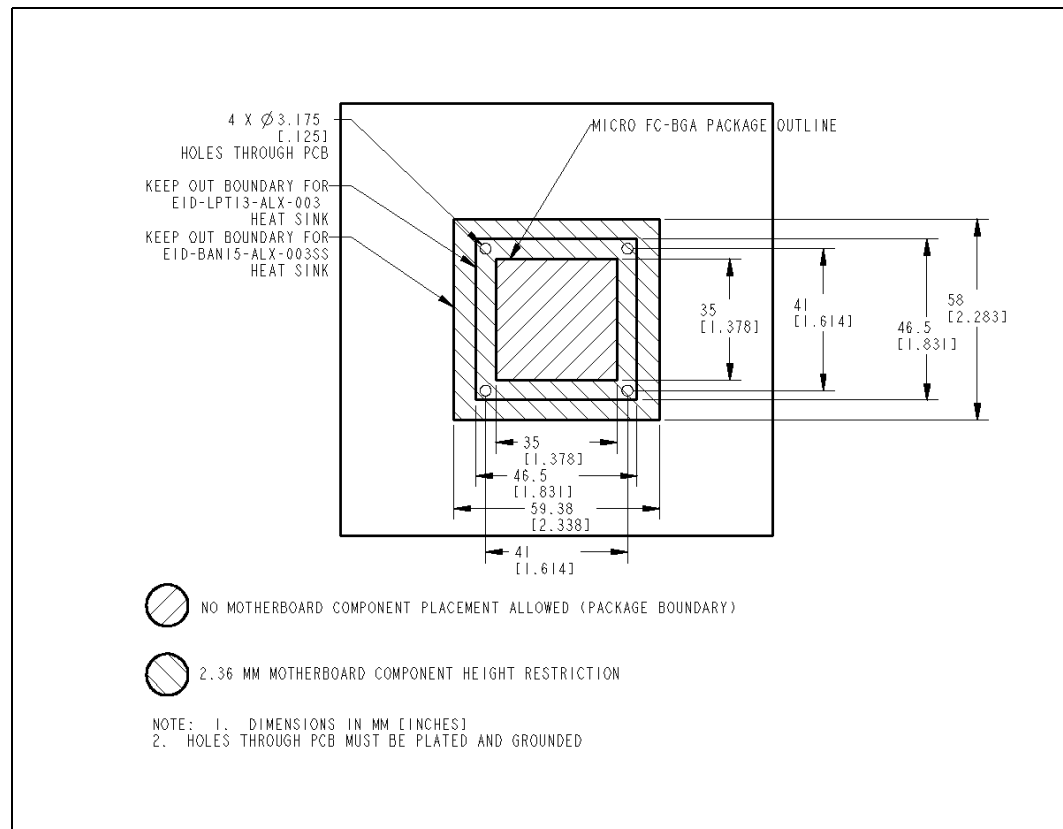
## 2.1.2 Volumetric Constraint Zones

The volumetric constraint zone reserved for the processor package, heat sink, and heat sink attachment method for the baseboard is shown in Figure 7 through Figure 11. There are multiple zones depending on which processor is being used:

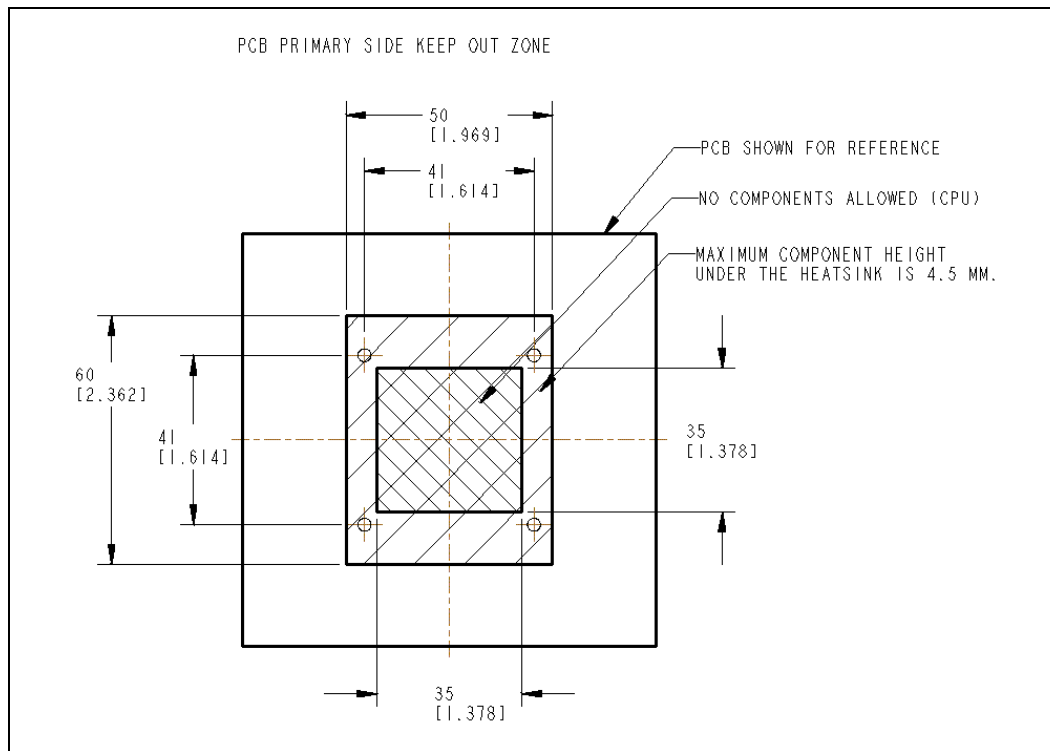
- Celeron M processor Ultra Low Voltage (ULV)
- Celeron M processor in the micro-FCBGA package
- Celeron M processor in the micro-FCPGA package

The volumetric constraint zone for the Celeron M processor for the third-party vendor enabled heat sinks are shown in Figure 28 and Figure 29. For information on the maximum component heights for the Single-slot CompactPCI\*, AdvancedMC\*, and the AdvancedTCA\* form factors, refer to the specifications at the PICMG web site: [www.picmg.org](http://www.picmg.org). For information on the 1U form factor maximum component heights, refer to the specification at [www.ssiforum.org](http://www.ssiforum.org).

**Figure 7. Recommended PCB Volumetric Constraint Zone for Intel® Celeron® M processor Ultra Low Voltage in the Single-slot CompactPCI\* Form Factor**



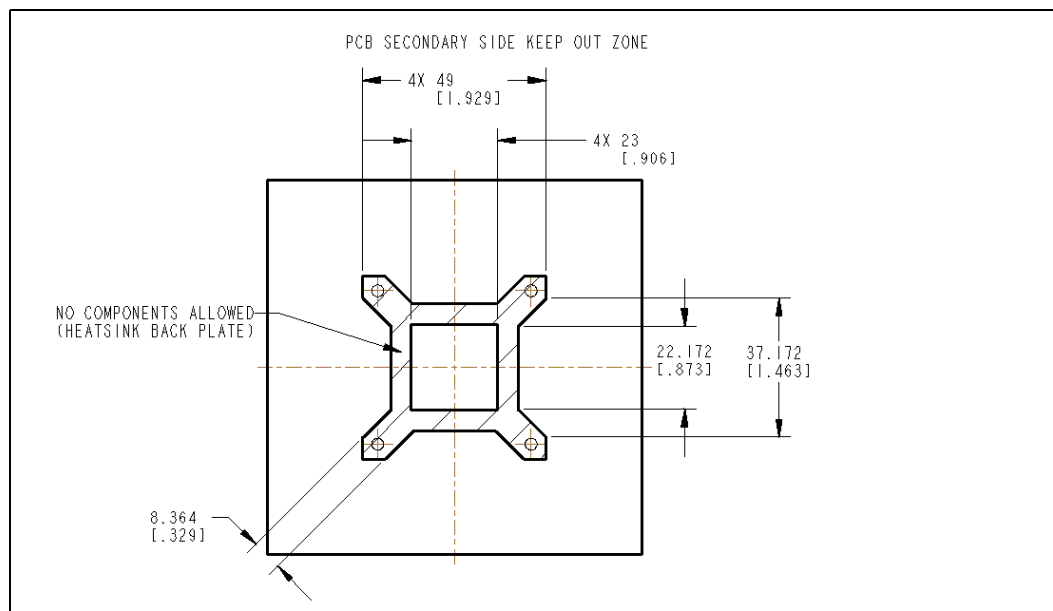
**Figure 8. Intel® Celeron® M processor Ultra Low Voltage Recommended PCB Volumetric Constraint Zone for the AdvancedMC\* on an AdvancedTCA\* Carrier Card (Primary Side)**



**NOTE:** Dimensions in mm [inches]

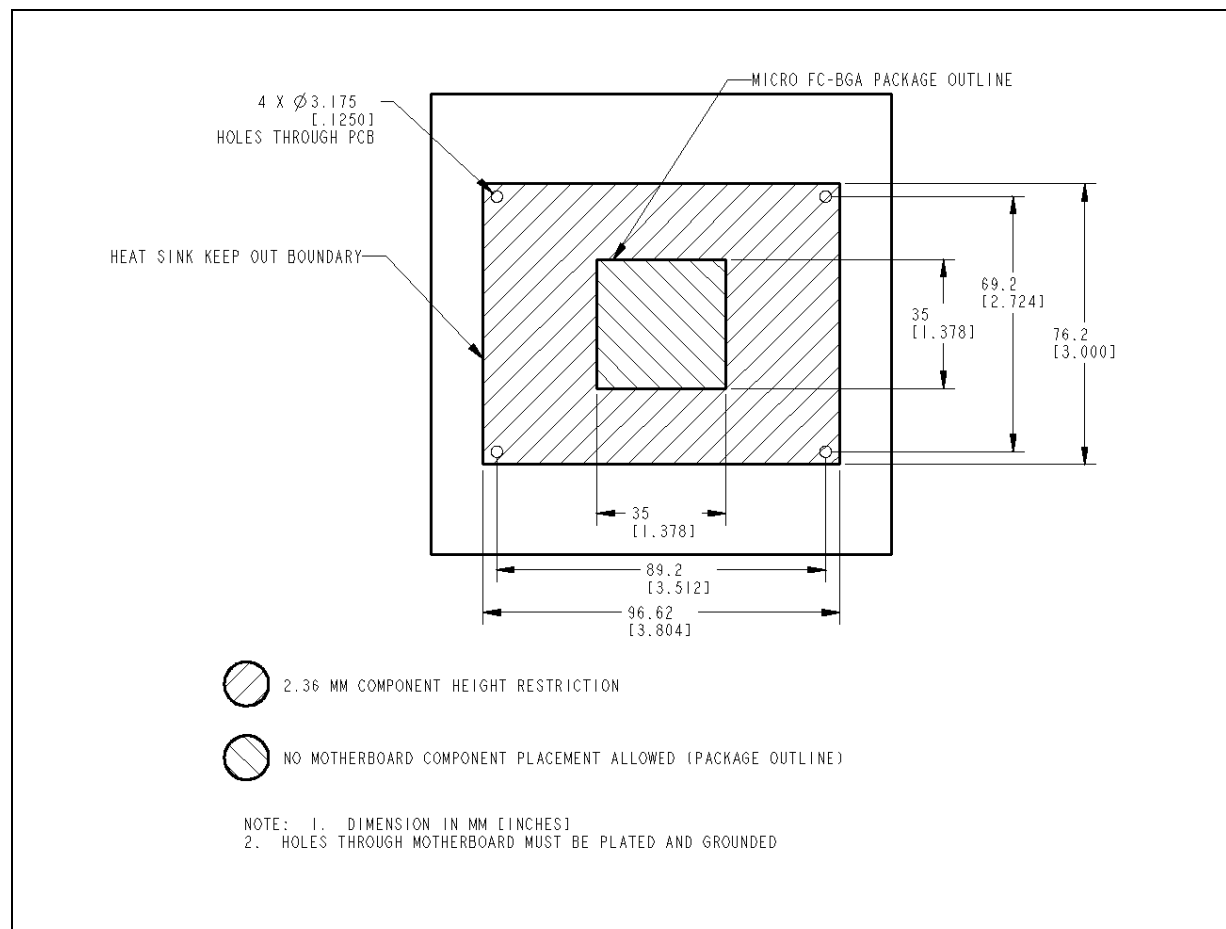


**Figure 9. Intel® Celeron® M processor Ultra Low Voltage Recommended PCB Volumetric Constraint Zone for the AdvancedMC\* on an AdvancedTCA\* Carrier Card (Secondary Side)**

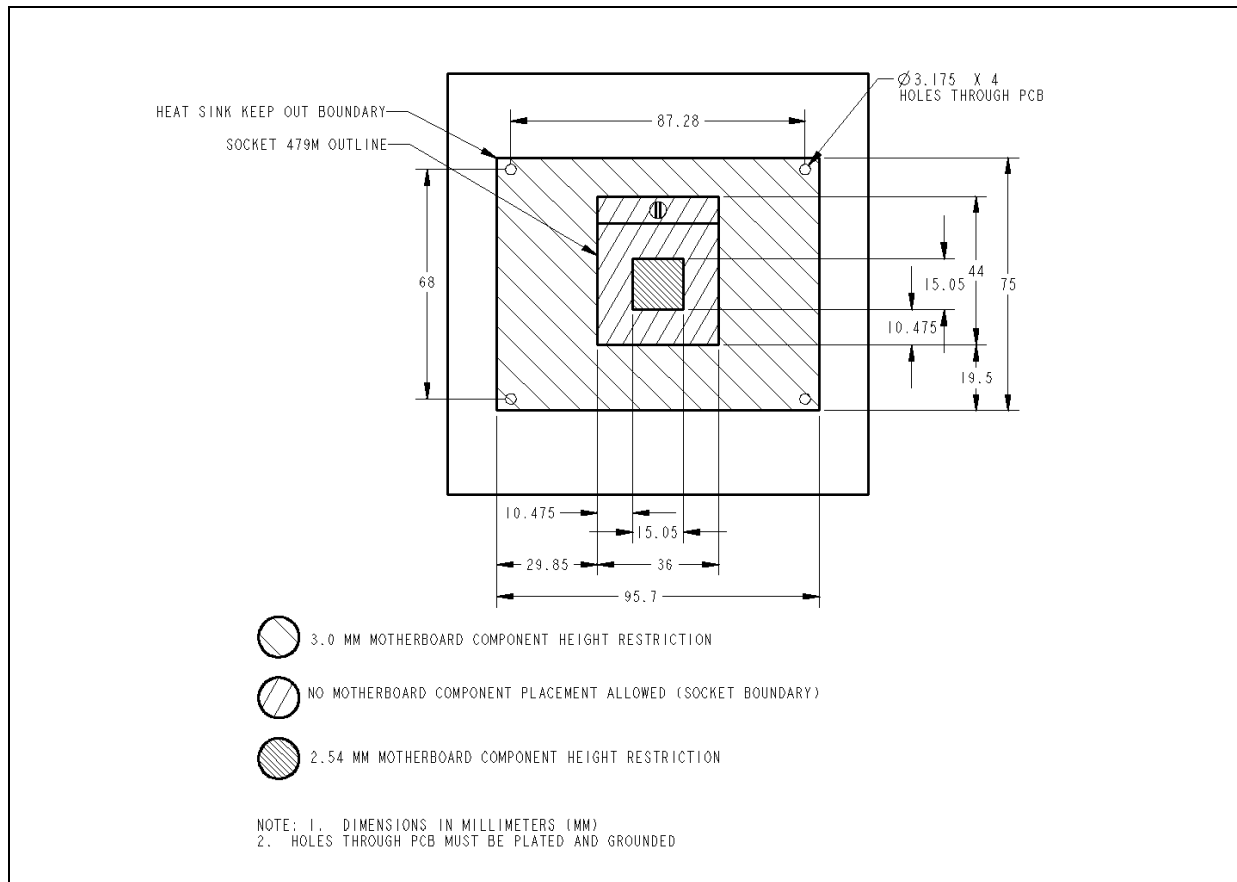


**NOTE:** Dimensions in mm [inches]

**Figure 10. Single-slot CompactPCI\* Form Factor Recommended PCB Volumetric Constraint Zone for the Intel® Celeron® M Processor in the micro-FCBGA Package**



**Figure 11. Single-slot CompactPCI\* Form Factor Recommended PCB Volumetric Constraint Zone for the Intel® Celeron® M Processor in the micro-FCPGA Package**



## 2.2 Thermal Guidelines

The performance of the thermal solution depends on many parameters, including the processor's:

- Thermal design power (TDP)
- Maximum junction temperature ( $T_{\text{junction-max}}$ )
- Operating ambient temperature
- System airflow

The guidelines and recommendations presented in this document are based on specific parameters. It is the responsibility of each product design team to verify that thermal solutions are suitable for their specific use.

To develop a reliable thermal solution all of the appropriate variables must be considered. Thermal simulations and characterizations must be carried out while accounting for all system parameters. The solutions presented in this document must be validated as specified in their final intended system.

Thermal data for the Celeron M processor and Celeron M processor ULV is presented in [Table 5](#). The data is provided for informational purposes only. Please refer to the processor's datasheet for the most current data. In the event of conflict, the processor's datasheet supersedes information provided in this document.

**Table 5. Thermal Specifications for the Intel® Celeron® M Processor and Ultra Low Voltage Intel® Celeron® M Processor**

Processor Number	Core Frequency (GHz)	Thermal Design Power (W)	Minimum T <sub>JUNCTION</sub> (°C)	Maximum T <sub>JUNCTION</sub> (°C)
370	1.5	21.0	0	100
373	1.0	5.5	0	100

## 2.2.1 Processor Power

The processor's power is specified as Thermal Design Power (TDP) for thermal solution design. TDP is defined as the worst-case power dissipated by the processor while executing publicly available software under normal operation conditions, at nominal voltages that meet the load line specifications. The Intel TDP specification is a recommended design point and is not representative of the absolute maximum power the processor may dissipate under worst case conditions. For any excursions beyond TDP, the Thermal Monitor feature is available to maintain the processor thermal specifications. Refer to the processor datasheet for details regarding the Thermal Design Power Specifications and the Thermal Monitor.

## 2.2.2 Thermal Diode

The Celeron M processor incorporates two methods of monitoring die temperature, the Intel Thermal Monitor and the thermal diode. The Intel Thermal Monitor must be used to determine when the maximum specified processor junction temperature has been reached. The second method, the thermal diode, may be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard, or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but cannot be used to indicate that the maximum T<sub>J</sub> of the processor has been reached. The thermal diode may only be used for long term, steady state measurement of die temperature. It is not suitable of real time thermal management. For more information refer to the *Intel® Celeron® M Processor on 90 nm Process Datasheet*.

**Note:** The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. Inaccuracies can include:

- the external thermal sensor
- on-die temperature gradients between the location of the thermal diode and the hottest location on the die
- time based variations in the die temperature measurement

Time based variations may occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T<sub>J</sub> temperature may change.

### 2.2.3 Intel Thermal Monitor

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the thermal control circuit (TCC): automatic mode and on demand mode. If both modes are activated, automatic mode takes precedence. **The Intel Thermal Monitor automatic mode must be enabled via BIOS for the processor to be operating within specifications.**

The automatic mode is called Intel Thermal Monitor 1. This mode is selected by writing values to the Model Specific Registers (MSRs) of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

When Intel Thermal Monitor 1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. After the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory-configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers or interrupt-handling routines. Processor performance is decreased by the same amount as the duty cycle when the TCC is active; however, with a properly designed and characterized thermal solution, the TCC most likely will never be activated, or only will be activated briefly during the most power intensive applications.

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor Control Register is written to a “1”, the TCC is activated immediately, independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor Control Register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/87.5% off, to 87.5% on/12.5% off, in 12.5% increments. on-demand mode may be used at the same time automatic mode is enabled; however, if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode takes precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

**Note:** PROCHOT# will not be asserted when the processor is in the Stop Grant, Sleep, Deep Sleep and Deeper Sleep low power states (internal clocks stopped), hence the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within the 100° C (maximum) specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above low-power states with PROCHOT# already asserted, PROCHOT# remains asserted until the processor exits the low power state and the processor junction temperature drops below the thermal trip point.

If automatic mode is disabled, the processor is operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor automatically shuts down when the silicon has reached a temperature of approximately 125° C. At this point, the FSB signal THERMTRIP# will go active. THERMTRIP# activation is

independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in the *Intel® Celeron® M Processor on 90 nm Process Datasheet*.

## 2.2.4 Power Density and Non-Uniform Heating

The Celeron M processor die does not exhibit an even power distribution over its surface area. Non-uniform power distributions may adversely affect the overall thermal solution performance. The thermal interface material, which functions as the first layer of heat spreading above the die, will be most susceptible to non-uniform die power characteristics.

The power density factor for the Celeron M processor will be higher than on previous processors. Processor thermal solution designers must account for the increase in expected thermal impedance (or resistance) from the thermal interface material when it is attached to the processor die. Processor heat sink performance will not be affected to the same degree as the TIM and is dependent on many factors, including heat sink size, base thickness, and material used. It is the responsibility of the OEM thermal solution designer to validate overall thermal solution performance.

## 2.2.5 Thermal Solution Requirements

The thermal solutions in this document were designed based on the processor thermal specifications as outlined in the processor's datasheet. The processor local ambient temperature for the Celeron M processor and the Celeron M processor ULV will vary depending on the thermal solution used and the amount of airflow provided. The performance charts for the reference heat sinks provide an estimated thermal resistance based on the amount of airflow provided. The ambient temperature and airflow are based on a measurement approximately one inch (25.4 mm) upstream from the processor.

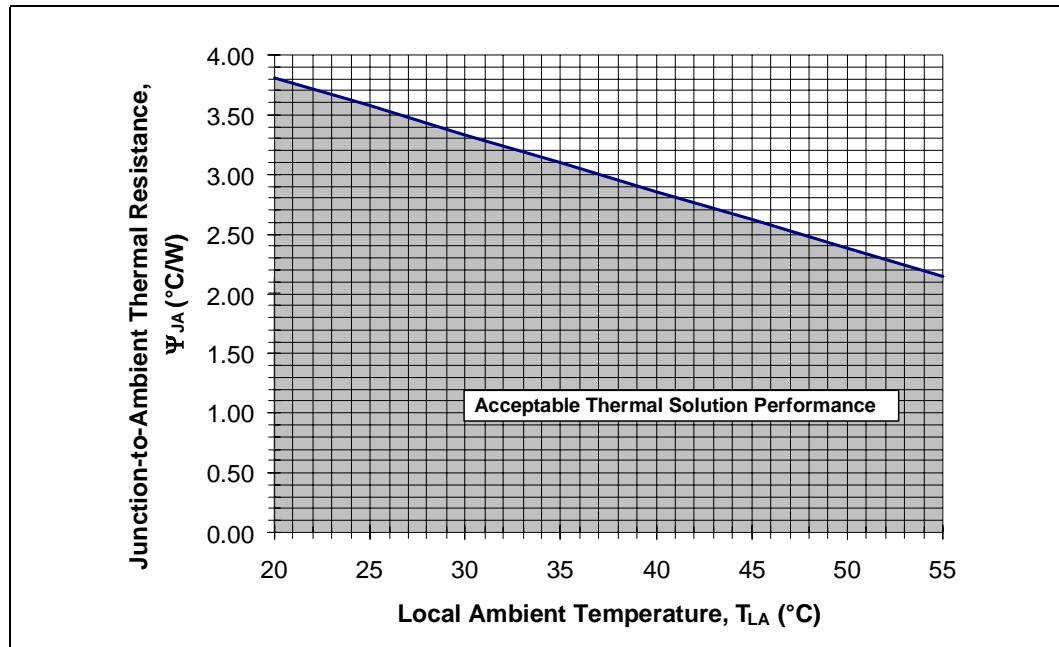
The thermal performance required for the heat sink is determined by calculating the junction-to-ambient thermal characterization parameter,  $\Psi_{JA}$ . This is a thermal engineering parameter that may be used to evaluate and compare different thermal solutions. For the Intel® Celeron® M Processor 370, an example of how  $\Psi_{JA}$  is calculated is shown in [Equation 1](#).

### Equation 1. Calculation of $\Psi_{JA}$

$$\Psi_{JA} = \frac{T_{Jmax}^{\circ C} - T_{LA}^{\circ C}}{TDP(W)} = \frac{100^{\circ C} - 50^{\circ C}}{21.0W} = 2.38 \frac{^{\circ C}}{W}$$

[Figure 12](#) further illustrates the required thermal performance for the Celeron M processor 370 at different operating ambient temperatures. The thermal solution used to cool the processor must have a junction-to-ambient thermal resistance less than or equal to the values shown for the given local ambient temperature. This same kind of chart can be created for the Celeron M processor ULV 373, to see what heatsink performance is needed at various ambient temperatures.

**Figure 12. Thermal Resistance Values for the Intel® Celeron® M Processor 370 at Various Local Ambient Operating Temperatures**



## 2.2.6 Recommended Heat Sink Designs

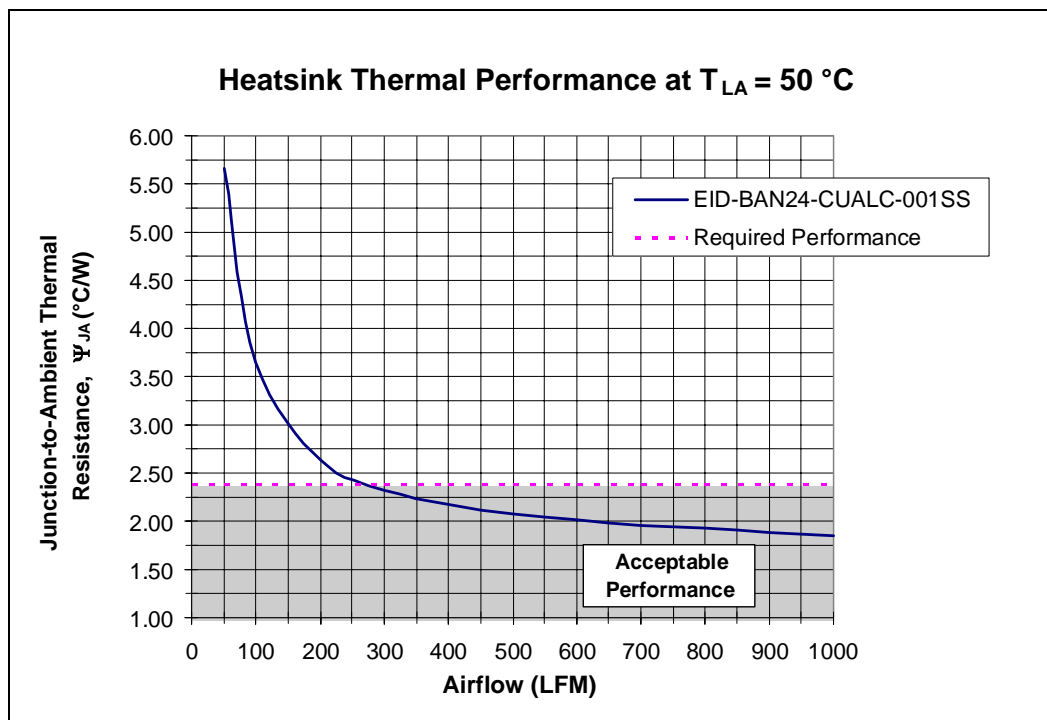
### 2.2.6.1 Intel® Celeron® M Processor in the Micro-FCBGA Package—Copper Base, Aluminum Fin Heat Sink #1

This heat sink was designed to meet the required thermal performance for a maximum local ambient temperature of 50° C. The heat sink shown in [Figure 22](#) was optimized using computational fluid dynamic (CFD) and thermal modeling software. The heat sink is optimized for a non-ducted airflow, as measured approximately one inch upstream from the processor.

[Figure 13](#) shows the thermal performance for the copper/aluminum heat sink in a non-ducted configuration.

Thermal modeling and lab verification tests indicate that this heat sink has a junction-to-ambient thermal resistance of 2.33° C/W with 300 LFM of system airflow, thus meeting the requirements of heat sink thermal performance for the Celeron M processor.

Figure 13. Intel® Celeron® M Processor Copper Base, Aluminum Fin  
Heat Sink #1 (EID-BAN24-CUALC-001SS) Thermal Performance Curve





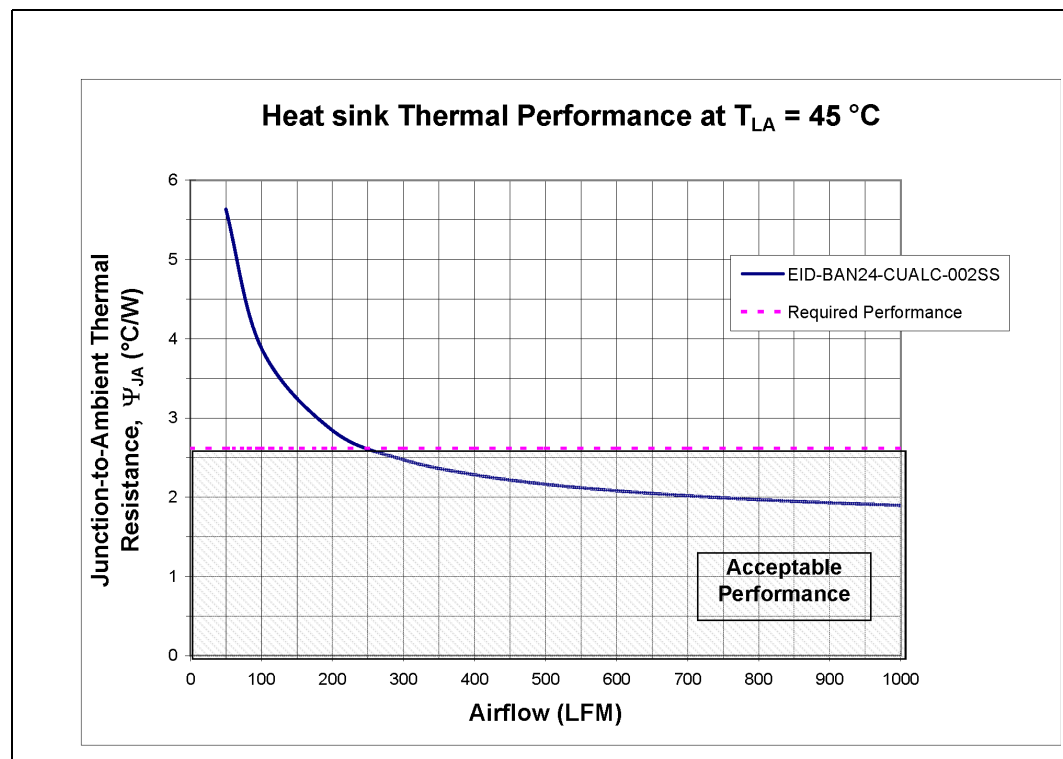
### 2.2.6.2 Celeron® M Processor in the Micro-FCPGA Package— Copper Base, Aluminum Fin Heat Sink #2

This heat sink was designed to meet the required thermal performance for a maximum local ambient temperature of 45° C. The heat sink shown in Figure 22 was optimized using computational fluid dynamic (CFD) and thermal modeling software. The heat sink is optimized for a non-ducted airflow, as measured approximately one inch upstream from the processor.

Figure 14 shows the thermal performance for the copper/aluminum heat sink in non-ducted configuration.

Thermal modeling and lab verification tests indicate that this heat sink has a junction-to-ambient thermal resistance of 2.47° C/W with 300 LFM of system airflow, thus meeting the requirements of heat sink thermal performance for the Celeron M processor.

**Figure 14. Intel® Celeron® M Processor Copper Base, Aluminum Fin Heat Sink #2 (EID-BAN24-CUALC-002SS) Thermal Performance Curve**



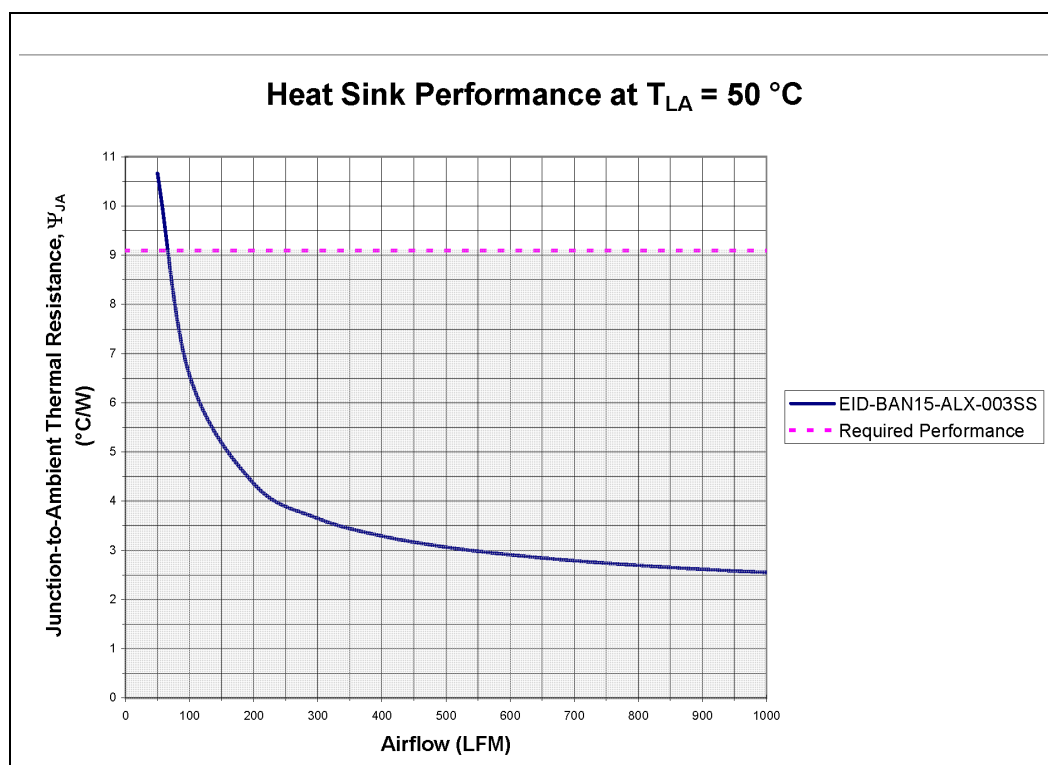
### 2.2.6.3 Celeron® M Processor ULV 373 in the Micro-FCBGA Package—Extruded Aluminum Heat Sink #1

This heat sink was designed to meet the required thermal performance for a maximum local ambient temperature of 50° C. The heat sink shown in Figure 24 was optimized using computational fluid dynamic (CFD) and thermal modeling software. The heat sink is optimized for a non-ducted airflow, as measured approximately one inch upstream from the processor.

Figure 15 shows the thermal performance for the extruded aluminum heat sink in non-ducted configuration.

Thermal modeling and lab verification tests indicate that this heat sink has a junction-to-ambient thermal resistance of 6.56° C/W with 100 LFM of system airflow, thus meeting the requirements of heat sink thermal performance for the Celeron M processor ULV.

**Figure 15. Celeron® M Processor ULV 373 Extruded Aluminum Heat Sink #1 (EID-BAN15-ALX-003SS) Thermal Performance Curve**



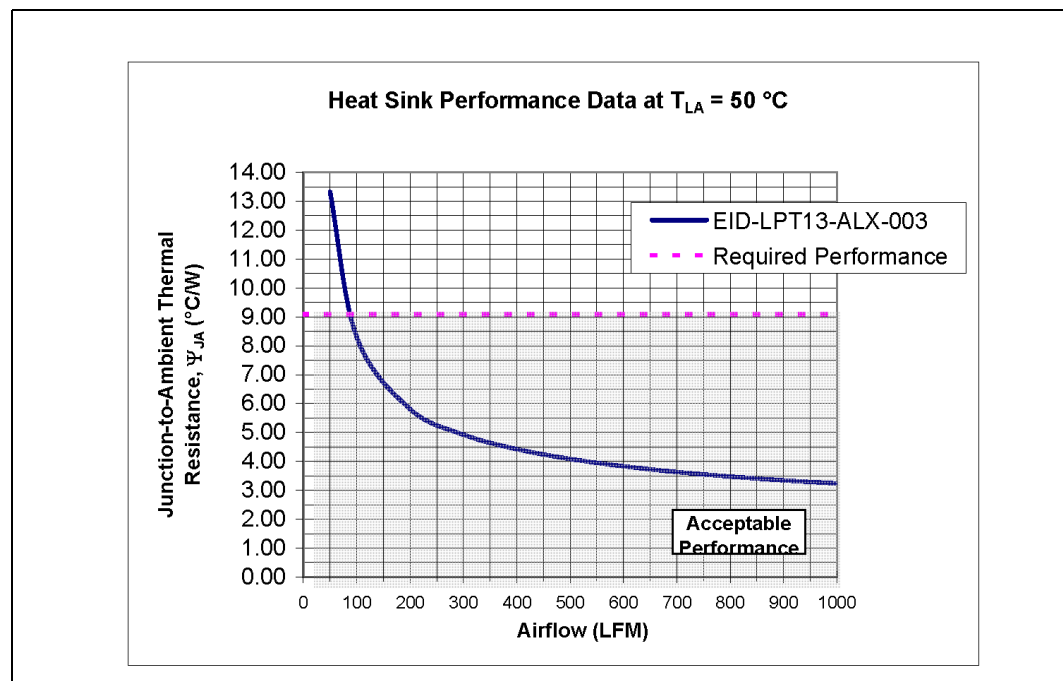
#### 2.2.6.4 Intel® Celeron® M Processor Ultra Low Voltage 373—Extruded Aluminum Heat Sink #2

This heat sink was designed to meet the required thermal performance for a maximum local ambient temperature of 50° C. The heat sink shown in Figure 25 was optimized using computational fluid dynamic (CFD) and thermal modeling software. The heat sink is optimized for a non-ducted airflow, as measured approximately one inch upstream from the processor.

Figure 16 shows the thermal performance for the extruded aluminum heat sink in non-ducted configuration.

Thermal modeling and lab verification tests indicate that this heat sink has a junction-to-ambient thermal resistance of 8.29° C/W with 100 LFM of system airflow, thus meeting the requirements of heat sink thermal performance for the Celeron M processor ULV.

**Figure 16. Intel® Celeron® M Processor Ultra Low Voltage 373 Extruded Aluminum Heat Sink #2 (EID-LPT13-ALX-003) Thermal Performance Curve**



### 2.2.6.5 Reference Heat Sink for the Intel® Celeron® M Processor Ultra Low Voltage 373 for the Advanced Mezzanine Card on an AdvancedTCA\* Carrier Card

The reference heat sink for the AdvancedMC\* form factor was designed to meet the thermal and mechanical constraints of the PICMG 3.0 specification. This copper heat sink, shown in [Figure 26](#) and [Figure 27](#), was optimized using a computational fluid dynamic (CFD) and thermal modeling software. The heat sink is optimized for non-ducted airflow, as measured approximately one inch upstream from the processor.

The maximum allowable local ambient temperature will vary depending on the amount of airflow provided.

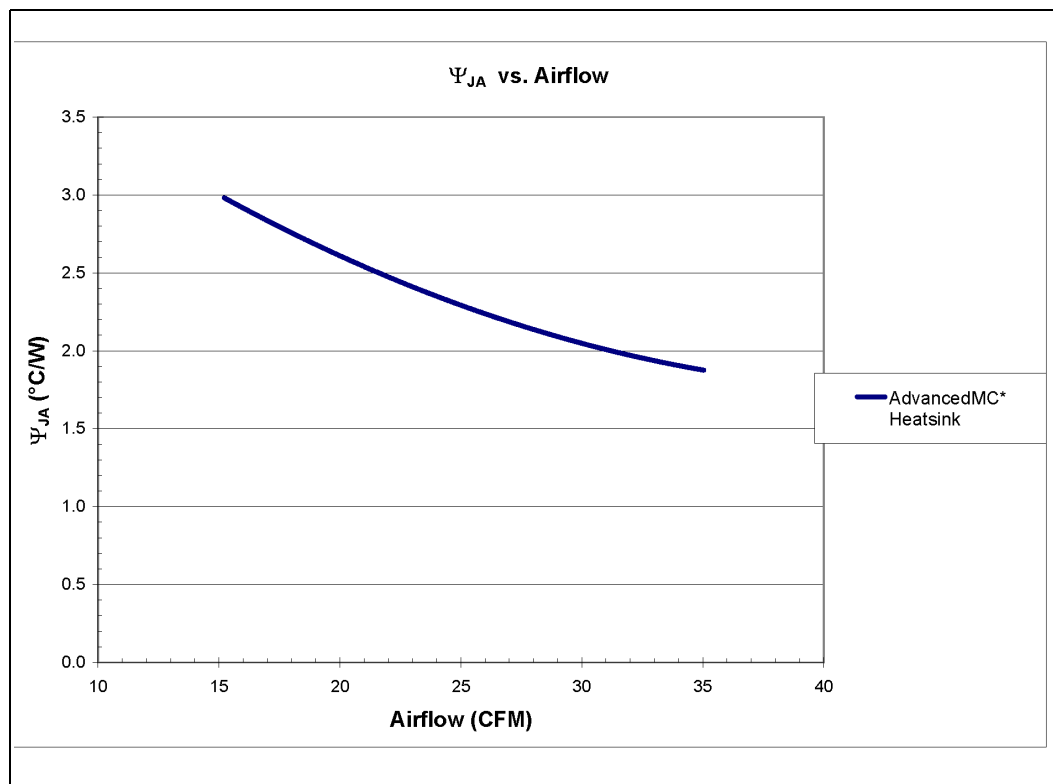
[Figure 17](#) shows the thermal performance of the heat sink at multiple airflow rates. It is important to note that the volumetric airflow shown in the figure is the amount of airflow in the AdvancedMC\* section of the AdvancedTCA\* board.

The performance of the heat sink shown in the figure, is the expected performance based on a Thermal Interface material at the End of Line performance. Over time the TIM material will degrade and the impedance of the material will increase. This increase in impedance will affect the performance of the thermal solution. It is recommended that system integrators work with their TIM suppliers to determine the performance of the material. This solution was tested with Honeywell\* PCM45F\* high performance phase change material.

This solution is attached to the PCB with the use of a backplate and spring loaded screws. The PCB volumetric constraint zones can be seen in [Figure 8](#) and [Figure 9](#).

The AdvancedMC\* heat sink was tested in lab verification tests to ensure that it is performing within expectations. It is up to the system integrators to perform full validation of the thermal solution including heat sink, TIM, and attach mechanism.

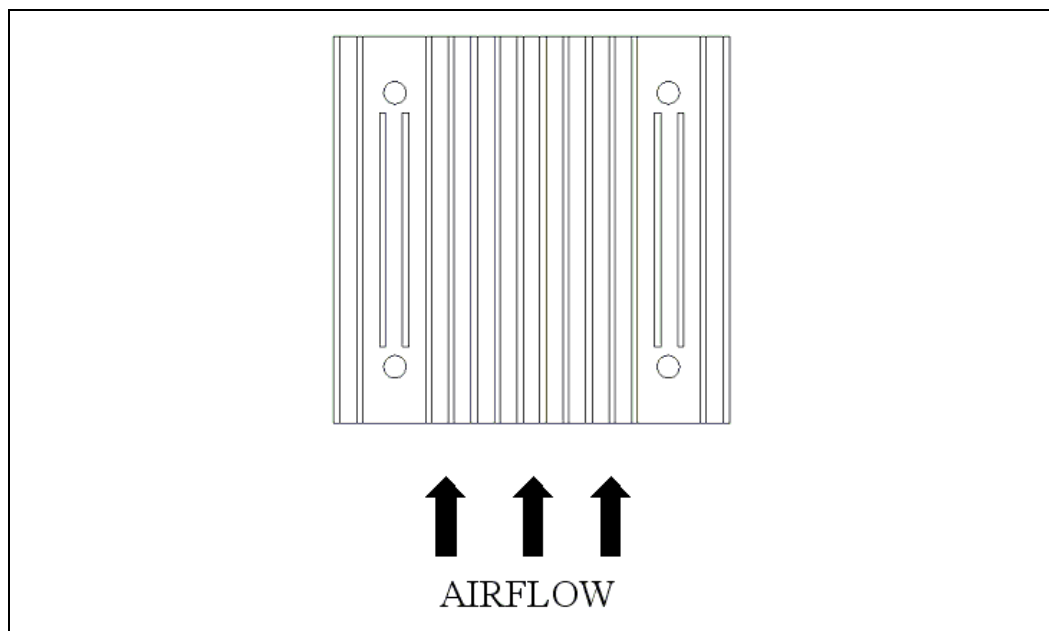
**Figure 17. Reference Heat Sink for the Celeron® M Processor Ultra Low Voltage 373 for the AdvancedMC\* on an AdvancedTCA\* Carrier Card, Thermal Performance Curve**



### 2.2.6.6 Heat Sink Orientation Relative to Airflow

The heat sinks were designed to maximize the available space within the volumetric constraint zone. These heat sinks must be oriented in a specific direction relative to the processor volumetric constraint zone and airflow. In order to use this design, the processor must be placed on the PCB in an orientation so the heat sink fins will be parallel to the airflow. [Figure 18](#) illustrates this orientation. A top view of the heat sink assembly is shown.

**Figure 18. Heat Sink Orientation Relative to Airflow Direction**



### 2.2.7 Thermal Interface Material (TIM)

It is important to understand and consider the impact the interface between the processor and heat sink base has on the overall thermal solution. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity must be selected to optimize the thermal solution.

It is important to minimize the thickness of the thermal interface material, commonly referred to as the bond line thickness. A large gap between the heat sink base and processor die yields a greater thermal resistance. The thickness of the gap is determined by the flatness of both the heat sink base and the die, plus the thickness of the thermal interface material, and the clamping force applied by the heat sink attachment method. To ensure proper and consistent thermal performance, the TIM and application process must be properly designed.

Thermal interface materials have a thermal impedance (resistance) that will increase over time as the material degrades. It is important for thermal solution designers to take this increase in impedance into consideration when designing a thermal solution. It is recommended that system integrators work with TIM suppliers to determine the performance of the desired thermal interface material. If system integrators wish to maintain maximum thermal solution performance, the TIM could be replaced during standard maintenance cycles.

The heat sink solutions were optimized using high-performance TIMs with low thermal impedance. The heat sinks were designed using ShinEtsu\* G751 thermal grease and Honeywell\* PCM45F phase change material. Vendor information for this material is provided in [“Vendor Information” on page 36](#). Alternative materials may be used at the user’s discretion. The entire heat sink assembly, including the heat sink, attach method, and thermal interface material, must be validated together for specific applications.

### **2.2.8 Recommended Thermal Solution Attachment Method**

The thermal solutions have been designed with mounting holes in the heat sink base. The fastening system that should be used consists of screws, springs, and backplate. To be used in a CompactPCI system, the system designer must conform to maximum component height specifications on both the primary and secondary sides of the PCB. The entire heat sink assembly must be validated together for specific applications, including the heat sink, attach method, and thermal interface material.

### **2.2.9 Intel® Celeron® M Processor Thermal Test Vehicle**

To aid in thermal design and validation, Intel has developed a thermal test vehicle (TTV) for the Celeron M processor. Using a TTV is the only recommended method for performing thermal solution validation. This is due to the fact that the amount of power can be controlled and measured, whereas on a real processor in a system, it is very difficult to accurately measure processor power dissipation. For more information contact your Intel field representative.

## 3.0 Third-Party Vendor Enabled Active Heat Sinks

This vendor list is provided as a service to our customers for reference only. The inclusion of this list should not be considered a recommendation or product endorsement by Intel Corporation.

### 3.1 Applications

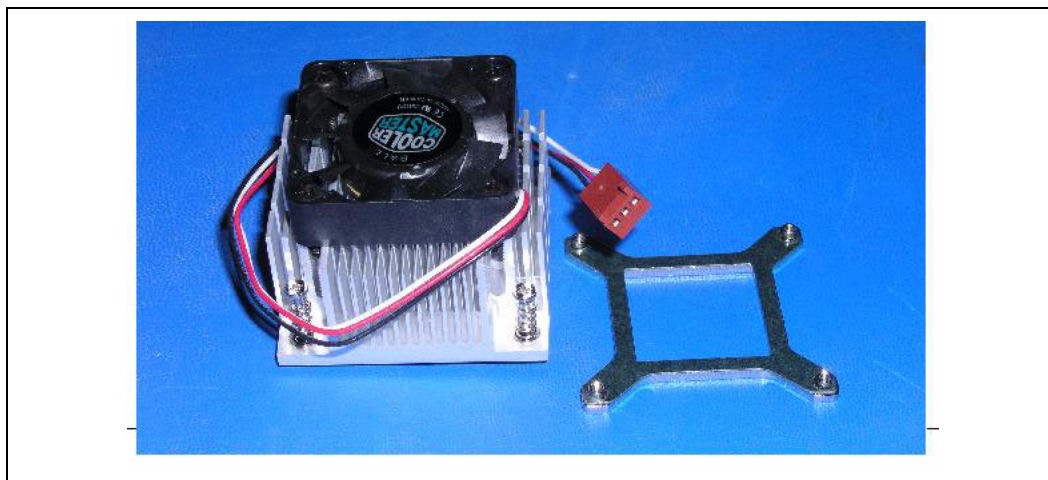
CoolerMaster® has developed a number of active fan heat sinks that can be used to provide cooling for the Celeron M processor for Embedded Applications. These heat sinks are a good fit for platforms requiring an active thermal solution (integrated fan heat sink) if z-height allows for 1U or greater of clearance. The following sections provide details on the different active fan sinks.

#### 3.1.1 EEP-N41ES-02 and EEB-N41ES-02

The following active heat sink was developed to minimize footprint on the motherboard while still providing an effective means to dissipate heat from processors in the micro-FCPGA and micro-FCBGA packages. The part number for this heat sink has either a P for micro-FCPGA package or a B for micro-FCBGA package.

This is an aluminum heat sink that has approximate dimensions of 50 mm x 50 mm x 35.5 mm. This heat sink is too tall for 1U server applications but is a good fit for form factors that have the available height.

**Figure 19. Active Aluminum Heat Sink, EEP-N41ES-02 and EEB-N41ES-02**



##### 3.1.1.1 Thermal Performance

Thermal performance for the heat sink was verified with the Celeron M TTV. The heat sink is capable of cooling a Celeron M processor at 21.0 W with local ambient temperatures up to  $T_{LA} = 64^{\circ}\text{C}$ . The performance of the thermal solution is a verification test only to ensure that the heat sink is performing within expectations. This test does not imply any statistical significance; it is up to system integrator to perform validation in the final intended system, including the heat sink, attach method, and thermal interface material.



**Table 6. Aluminum Active Heat Sink Thermal Performance**

Thermal Performance (° C/W)	$\Psi_{JA} = 1.67^{\circ} \text{ C/W}$
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### 3.1.1.2 Mechanical Retention and Volumetric Constraint Zones

The active heat sink is attached to the motherboard using a backplate that is fastened to the motherboard by four screws. This attach method uses spring-loaded fasteners to apply an even load on the processor die. The backplate, when assembled, will be flush against the backside of the motherboard.

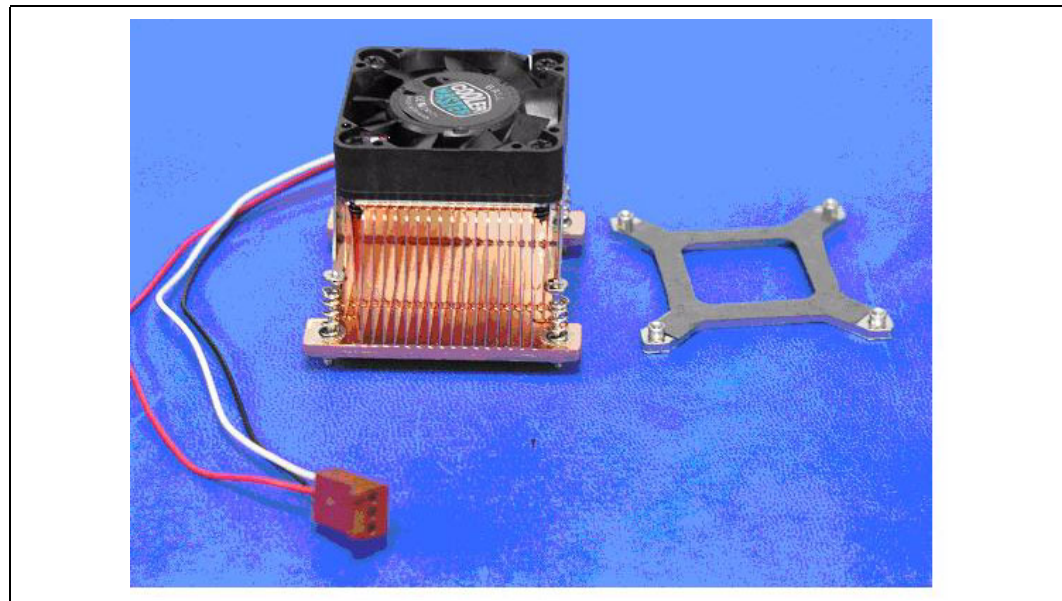
The volumetric constraint zone for this heat sink is shown in Figure 28 and Figure 29. Figure 28 shows the primary side volumetric constraint for processors in the micro-FCPGA and micro-FCBGA packages. This drawing is based on the standard mobile Intel processor hole mounting pattern of 41 mm x 41 mm. Figure 29 shows the secondary side volumetric constraint zone for backplate assembly. It is important to adhere to both the primary and secondary side volumetric constraint zones so that there will be no interference with the assembly of the heat sink onto the motherboard.

### 3.1.2 EEP-N41CS-01 and EEB-N41CS-01

The following active heat sink was developed to minimize footprint on the motherboard while still providing an effective means to dissipate heat from processors in the micro-FCPGA and micro-FCBGA packages. The part number for this heat sink has either a P for Micro-FCPGA package or a B for Micro-FCBGA package.

This is a copper heat sink that has approximate dimensions of 50 mm x 50 mm x 40.5 mm. This heat sink is too tall for 1U server applications but is a good fit for form factors that have the available height.

**Figure 20. Active Copper Heat Sink, EEP-N41CS-01 and EEB-N41CS-01**



### 3.1.2.1 Thermal Performance

Thermal performance for the heat sink was verified with the Celeron M TTV. The heat sink is capable of cooling a Celeron M processor at 21.0 W with local ambient temperatures up to  $T_{LA} = 68^{\circ}\text{C}$ . The performance of the thermal solution is a verification test only to ensure that the heat sink is performing within expectations. This test does not imply any statistical significance; it is up to system integrator to perform validation in the final intended system, including the heat sink, attach method, and thermal interface material.

**Table 7. Active Copper Heat Sink Thermal Performance**

Thermal Performance ( $^{\circ}\text{C/W}$ )	$\Psi_{JA} = 1.52^{\circ}\text{C/W}$
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### 3.1.2.2 Mechanical Retention and Volumetric Constraint Zones

The active heat sink is attached to the motherboard using a backplate that is fastened to the motherboard by four screws. This attach method uses spring-loaded fasteners to apply an even load on the processor die. The backplate, when assembled, will be flush against the backside of the motherboard.

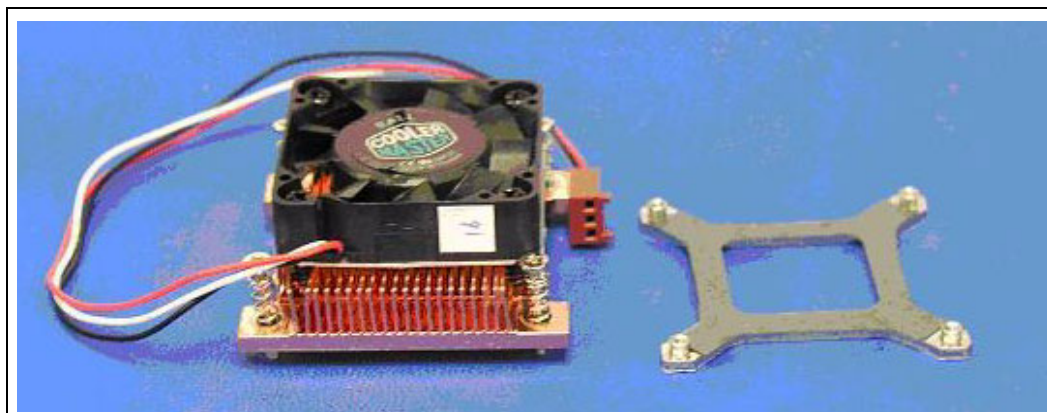
The volumetric constraint zone for this heat sink is shown in Figure 28 and Figure 29. Figure 28 shows the primary side volumetric constraint zone, including processors in the micro-FCPGA and micro-FCBGA packages. This drawing is based on the standard mobile Intel processor hole mounting pattern of 41 mm x 41 mm. Figure 29 shows the secondary side volumetric constraint zone for backplate assembly. It is important to adhere to both the primary and secondary side volumetric constraint zones so that there will be no interference with the assembly of the heat sink onto the motherboard.

### 3.1.3 EEP-N41SS-01 and EEB-N41SS-01

The following active heat sink was developed to minimize footprint on the motherboard while still providing an effective means to dissipate heat from processors in the micro-FCPGA and micro-FCBGA packages. The part number for this heat sink has either a P for Micro-FCPGA package or a B for Micro-FCBGA package.

This is a copper heat sink that has approximate dimensions of 50 mm x 50 mm x 23 mm. This heat sink is ideal for 1U or larger form factors that require the use of an active fan sink.

**Figure 21. Copper Active Heat Sink, EEP-N41SS-01 and EEB-N41SS-01**



### 3.1.3.1 Thermal Performance

Thermal performance for the heat sink was verified with the Celeron M TTV. The heat sink is capable of cooling a Celeron M processor at 21.0 W with local ambient temperatures up to  $T_{LA} = 60^{\circ}\text{C}$ . The performance of the thermal solution is a verification test only to ensure that the heat sink is performing within expectations. This test does not imply any statistical significance; it is up to system integrator to perform validation in the final intended system, including the heat sink, attach method, and thermal interface material.

**Table 8. Copper Active Heat Sink Thermal Performance**

Thermal Performance ( $^{\circ}\text{C/W}$ )	$\Psi_{JA} = 1.89^{\circ}\text{C/W}$
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### 3.1.3.2 Mechanical Retention and Volumetric Constraint Zones

The active heat sink is attached to the motherboard using a backplate that is fastened to the motherboard by four screws. This attach method uses spring loaded fasteners to apply an even load on the processor die. The backplate, when assembled, will be flush against the backside of the motherboard.

The volumetric constraint zone for this heat sink is shown in [Figure 28](#) and [Figure 29](#). [Figure 28](#) shows the primary side volumetric constraint zone, including processors in the micro-FCPGA and micro-FCBGA packages. This drawing is based on the standard mobile Intel processor hole mounting pattern of 41 mm x 41 mm. [Figure 29](#) shows the secondary side volumetric constraint zone for backplate assembly. It is important to adhere to both the primary and secondary side volumetric constraint zones so that there will be no interference with the assembly of the heat sink onto the motherboard.

## 3.2 Thermal Interface Material and Considerations

The CoolerMaster\* active heat sinks are delivered with preapplied thermal interface material. This material, Powerstrate\* 51, manufactured by Power Devices\*, Inc., is a phase-change thermal interface material. This implies the material will change properties at elevated temperatures to increase thermal performance. This phase change must be accounted for when testing the CoolerMaster active heat sink. At low temperatures, the heat sink performance will be significantly degraded, but at elevated junction temperatures, the material will change phase and improve in performance. For more information, see the Power Devices website at: <http://www.powerdevices.com>.

## 4.0 Vendor Information

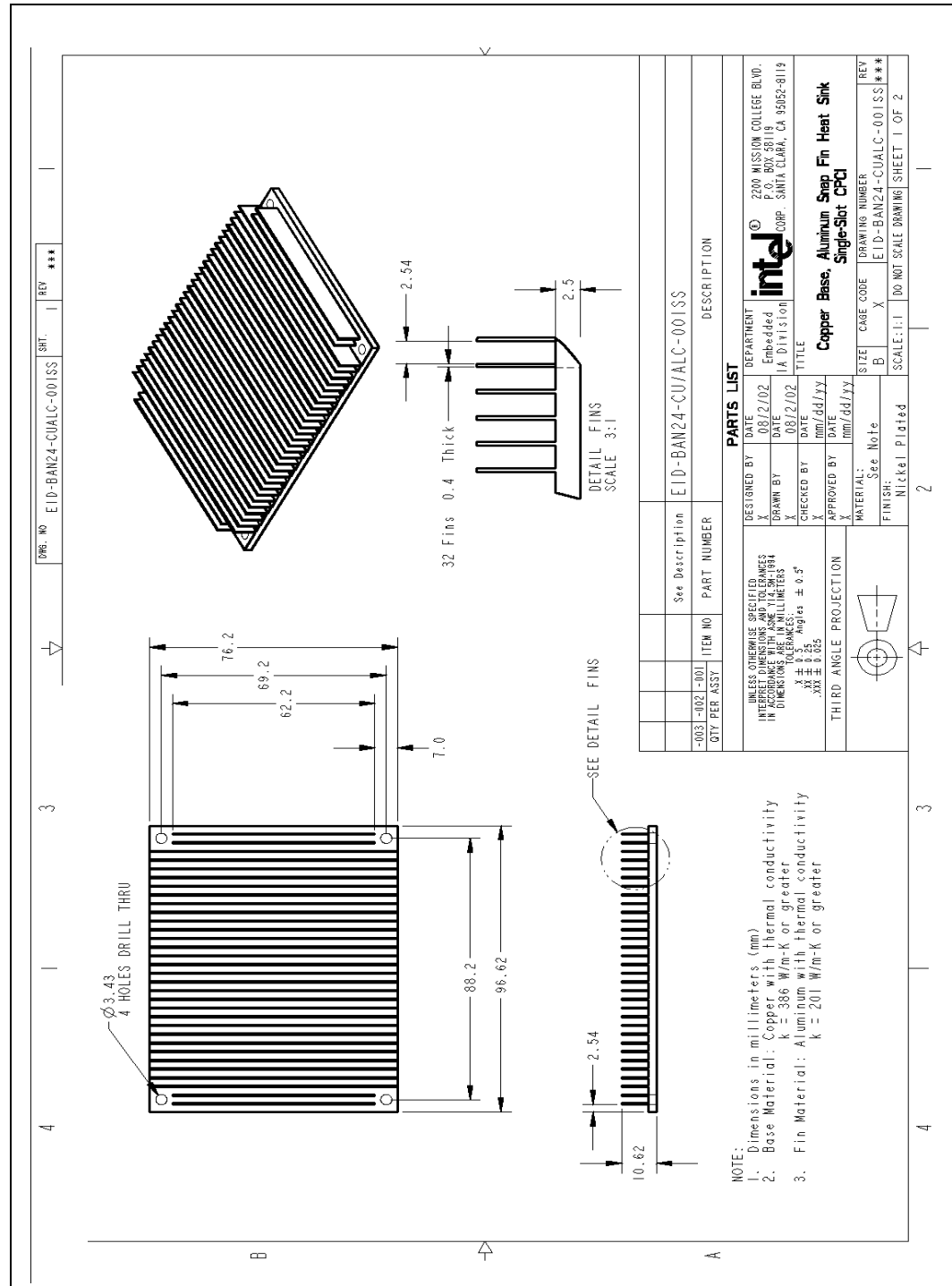
**Table 9. Vendor Contact Information†**

Supplier	Contact	Phone	E-mail	Components
Cooler Master 4124 Clipper Court Fremont, CA 94538 USA	Wendy Lin	510-770-8566 extension 211	wendy@coolermaster.com	<b>Extruded Aluminum Heat Sink, Reference No.</b> EID-BAN15-ALX-003SS and EID-LPT13-ALX-003 <b>Copper Base, Aluminum Snap Fin Heat Sink, Reference No.</b> EID-BAN24-CU/ALC-001SS and EID-BAN24-CU/ALC-002SS <b>Active Heat Sink, Part No.</b> Micro-FCPGA Package: EEP-N41ES-02, EEP-N41CS-01, EEP-N41SS-01 Micro-FCBGA Package: EEB-N41ES-02, EEB-N41CS-01, EEB-N41SS-01 <b>AdvancedMC* Reference Heat Sink</b> Assembly: ECC-00155-01 Heat sink only: 2500013570
Fujikura America Inc. 3001 Oakmead Village Dr. Santa Clara, CA 95051-0811	Ash Ooe	408-748-6991	a_ooe@fujikura.com	<b>Extruded Aluminum Heat Sink, Reference No.</b> EID-BAN15-ALX-003SS and EID-LPT13-ALX-003 <b>Copper Base, Aluminum Snap Fin Heat Sink, Reference No.</b> EID-BAN24-CU/ALC-001SS and EID-BAN24-CU/ALC-002SS
Shin-Etsu Micro Si, Inc. 10028 S. 51st St. Phoenix, AZ 85044		480- 893-8898	<a href="http://www.microsi.com">http://www.microsi.com</a>	Thermal Interface Material (ShinEtsu PN G751)
Power Devices Inc. 26941 Cabot Rd., Bldg. 124 Laguna Hills, CA 92653		949-582-6712	<a href="http://www.powerdevices.com">http://www.powerdevices.com</a>	Thermal Interface Material (Powerstrate* 51)
Honeywell*	Paula Knoll	858-279-2956	paula_knoll@honeywell.com	Thermal Interface Material, P/N PCM45F

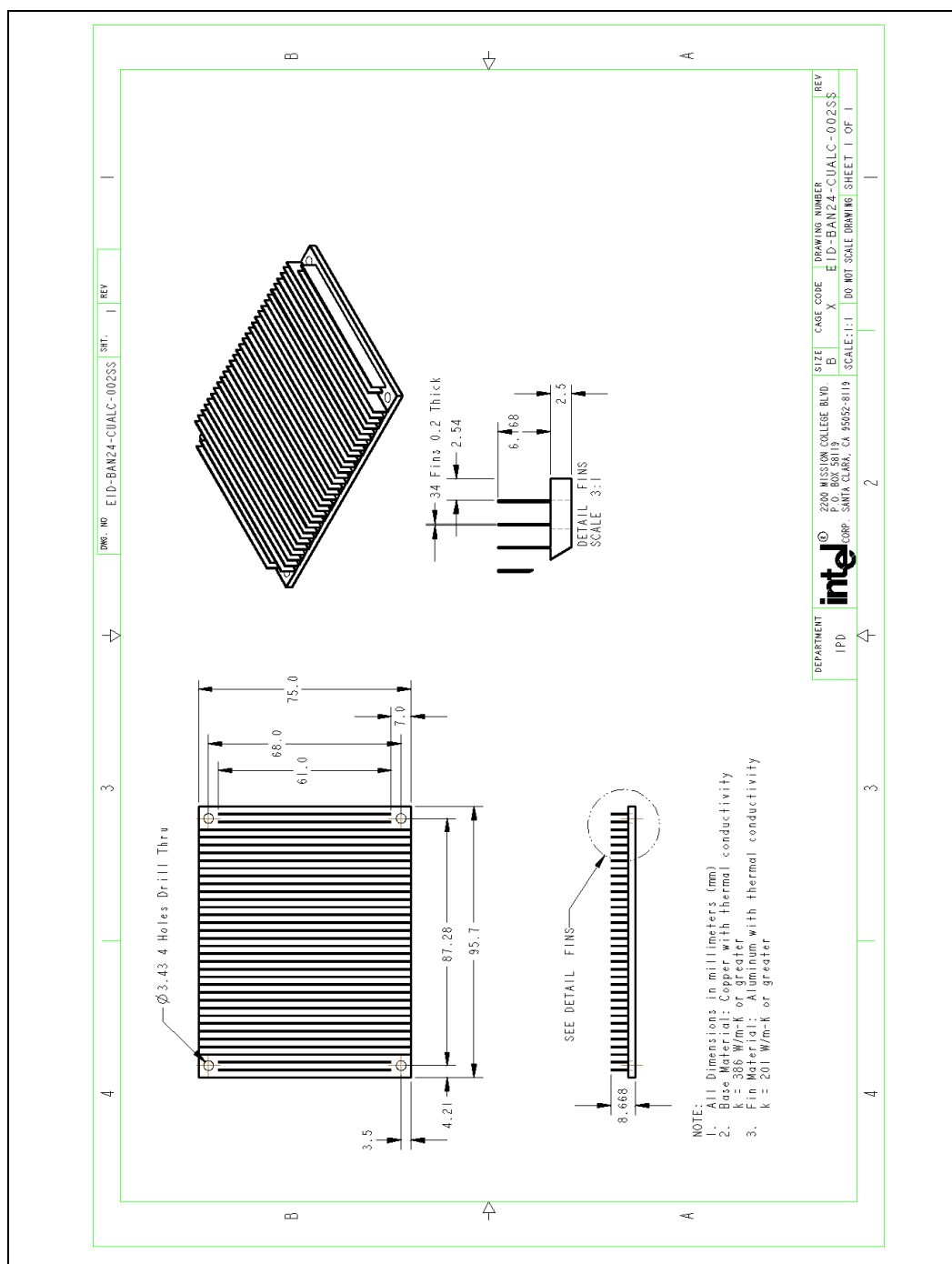
† This list is provided for convenience. Intel does not endorse third party vendor products. The designer is responsible for verifying compatibility with Intel products.

## Appendix A Heat Sink Mechanical Drawings

Figure 22. Intel® Celeron® M Processor in the Micro-FCBGA Package Heat Sink #1 (EID-BAN24-CUALC-001SS)



**Figure 23. Intel® Celeron® M Processor in the Micro-FCPGA Package Heat Sink #2 (EID-BAN24-CUALC-002SS)**

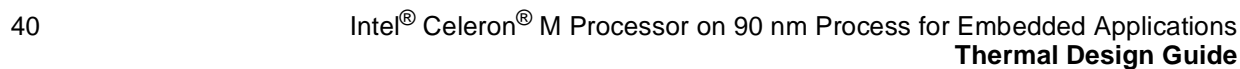


# Intel® Celeron® M Processor on 90 nm Process for Embedded Applications

## Thermal Design Guide



40 Intel® Celeron® M Processor on 90 nm Process for Embedded Applications  
**Thermal Design Guide**





# Intel® Celeron® M Processor on 90 nm Process for Embedded Applications

## Thermal Design Guide



42

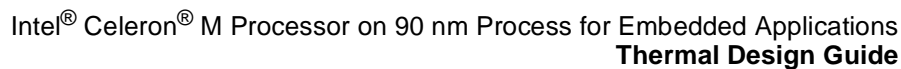




Figure 29. Active Heat Sink Volumetric Constraint Zone (Secondary Side)

